A fully-integrated 12.5-Gb/s 850-nm CMOS optical receiver based on a spatially-modulated avalanche photodetector

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Abstract: We present a fully integrated 12.5-Gb/s optical receiver fabricated with standard 0.13-μm complementary metal-oxide-semiconductor (CMOS) technology for 850-nm optical interconnect applications. Our integrated optical receiver includes a newly proposed CMOS-compatible spatially-modulated avalanche photodetector, which provides larger photodetection bandwidth than previously reported CMOS-compatible photodetectors. The receiver also has high-speed CMOS circuits including transimpedance amplifier, DC-balanced buffer, equalizer, and limiting amplifier. With the fabricated optical receiver, detection of 12.5-Gb/s optical data is successfully achieved at 5.8 pJ/bit. Our receiver achieves the highest data rate ever reported for 850-nm integrated CMOS optical receivers.

OCIS codes: (250.1345) Avalanche photodiodes (APDs); (250.3140) Integrated optoelectronic circuits; (200.4650) Optical interconnects; (230.0230) Optical devices; (250.0250) Optoelectronics; (230.5160) Photodetectors; (230.5170) Photodiodes; (040.6040) Silicon.

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1. Introduction

Optical interconnects are receiving a great amount of attention as a technique to overcome the fundamental limitations of electrical interconnects with possibilities for larger bandwidth, smaller size, and lower power consumption [1–5]. There are many efforts to realize optical interconnects for various applications. As one of these, low-cost 850-nm optical interconnects based on vertical-cavity surface-emitting lasers and multimode fibers are finding increasing ranges of applications such as home networks [6], communications in vehicles and airplanes [7], rack-to-rack interconnects within data centers and computer clusters [8], [9], and on-board interconnects [8–13]. 850-nm optical receivers that include monolithically integrated silicon photodetectors (PDs) and complementary metal-oxide-semiconductor (CMOS) electronics are particularly attractive since they have great cost benefits provided by CMOS technology as well as improved performance due to elimination of parasitic pad capacitances and bonding wire inductances that are unavoidable in hybrid approaches [14–20].

Several integrated optical receivers based on standard CMOS technology (CMOS-Rxs) have been reported [14–21]. The most critical issue for realizing high-performance CMOS-Rxs is development of high-performance CMOS-compatible silicon photodetectors (CMOS-PDs). CMOS-PDs realized with standard CMOS technology are typically very slow due to slow diffusion photocurrents produced in the substrate as 850-nm light has much longer penetration depth than the narrow depletion regions possible in standard CMOS technology. Several approaches have been tried to overcome this limitation [17–19], [22–27]. Recently, a 10-Gb/s CMOS-Rx was reported with a high-speed spatially-modulated PD (SM-PD) [18]. This SM-PD shows enhanced photodetection bandwidth by subtracting the diffusion photocurrents in one region from another. We also have previously reported a 10-Gb/s CMOS-Rx based on a CMOS-compatible avalanche photodetector (CMOS-APD) [21]. The CMOS-APD provides large photodetection bandwidth as well as enhanced responsivity [26], [27]. In [27], we identified that the photodetection bandwidth limiting factor of the CMOS-APD based on the P^+/N-well junction is the diffusion transit time of holes photogenerated in

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the N-well region. In this paper, we demonstrate that a higher-speed fully-integrated CMOS-Rx can be realized by employing a spatially-modulated CMOS-APD (SM-APD) that reduces the influence of hole diffusion. Detection of 12.5-Gb/s optical data is successfully achieved with the CMOS-Rx, which is the highest data rate reported for CMOS-Rxs until now.

2. Photodetector

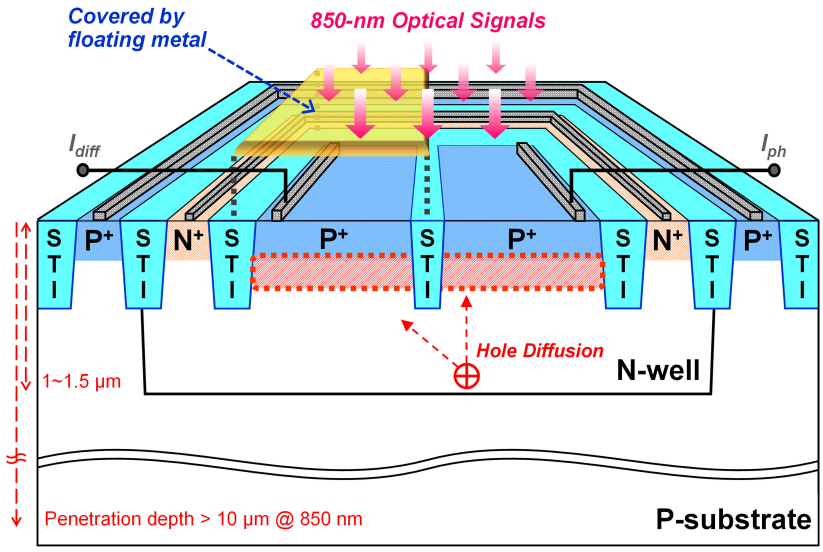

Fig. 1. Structure of the fabricated SM-APD.

Figure 1 shows the structure of the SM-APD used in our investigation. The SM-APD is fabricated with standard 0.13-μm CMOS technology without any design or layout rule violations. Although the N^+/P-well CMOS-APD has higher photodetection bandwidth than the P^+/N-well CMOS-APD [26], the present investigation is based on P^+/N-well junction photodetectors since the standard 0.13-μm CMOS technology on which our present investigation is based does not support the deep N-well layer required for N^+/P-well photodetectors. It has a total active area of 10 μm × 10 μm. The P^+ region is divided into two isolated regions by shallow trench isolation (STI), where one region is covered with a light-blocking metal layer. Photocurrents are extracted from P^+ contacts, I_{diff} from the covered region and I_{ph} from the uncovered region. Although there is no light incident into the covered region, there are holes diffused from the uncovered region. By subtracting I_{diff} from I_{ph}, slow diffusive components in the photocurrents can be eliminated. Unlike previously reported SM-PDs where diffusion currents in the substrate are eliminated by spatial modulation [17], [18], our structure eliminates those in the N-well. For optical-window formation, the self-aligned silicide (salicide) process is blocked. STI is used as a guard ring for the APD as it provides high gain without premature edge breakdown [28].

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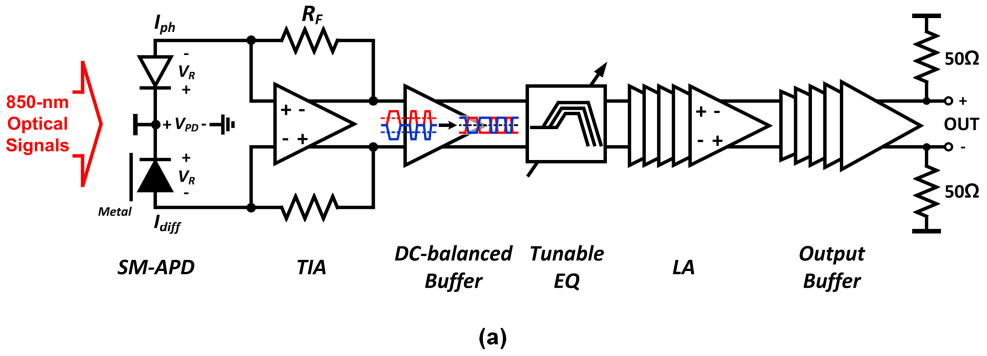
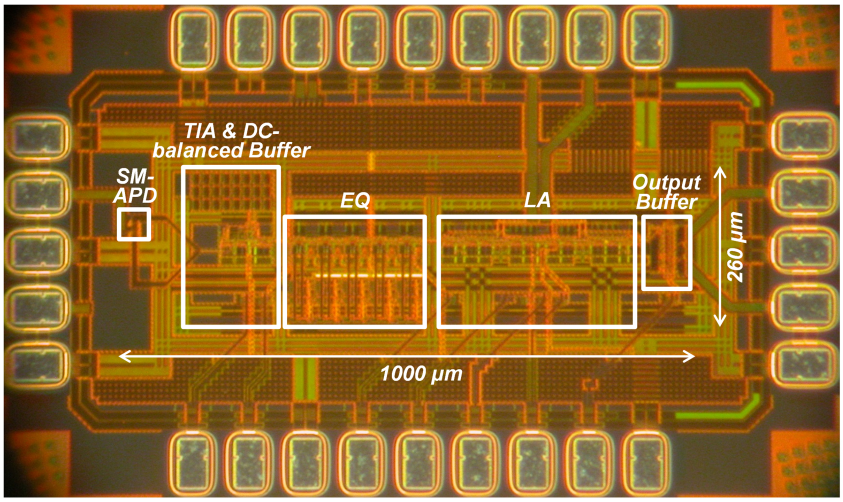
3. Integrated CMOS optical receiver



(a)



(b)

Fig. 2. (a) CMOS-Rx based on the proposed SM-APD. (b) Chip microphotograph.

The advantage of photodetectors realized in standard CMOS technology is that it can be monolithically integrated with powerful CMOS circuits. In order to demonstrate this, the SM-APD is integrated with CMOS receiver circuits. Figure 2(a) shows a simplified block diagram of the fabricated CMOS-Rx. It is composed of SM-APD, transimpedance amplifier (TIA) with DC-balanced buffer, tunable equalizer (EQ), limiting amplifier (LA), and output buffer with 50-Ω load. The TIA is designed in shunt-feedback configuration composed of two-stage common-source differential amplifiers with high feedback resistance of 4 kΩ. We can realize a high-speed and low-noise TIA relatively easily due to the low capacitance provided by the integrated SM-APD. The DC-balanced buffer converts pseudo-differential TIA output signals into fully-differential signals. It consists of two low-pass filters and a f_T-doubler. The EQ is designed to compensate the limited bandwidth of the TIA and DC-balanced buffer and consists of five stages of differential amplifiers with source degeneration and negative capacitance. EQ boosting gain can be changed with a tunable capacitor array. The LA is composed of five-stage gain cells that are interleaved to achieve the broadband and flat response. The output buffer is added so that it can drive 50-Ω load provided by the instruments used for measurements. Further details of the receiver circuits can be found in [21]. The microphotograph of the fabricated CMOS-Rx is shown in Fig. 2(b). Its core area is 1000 µm × 260 µm. SM-APD is connected to the TIA through two separate current paths, one for I_{ph} and the other for I_{diff}. There is a length difference of 80 µm between these two since

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SM-APD could not be placed in the middle due to V_{DD} and ground connections for the receiver circuit. However, this should not affect our 12.5 Gbps receiver performance.

4. Experimental results

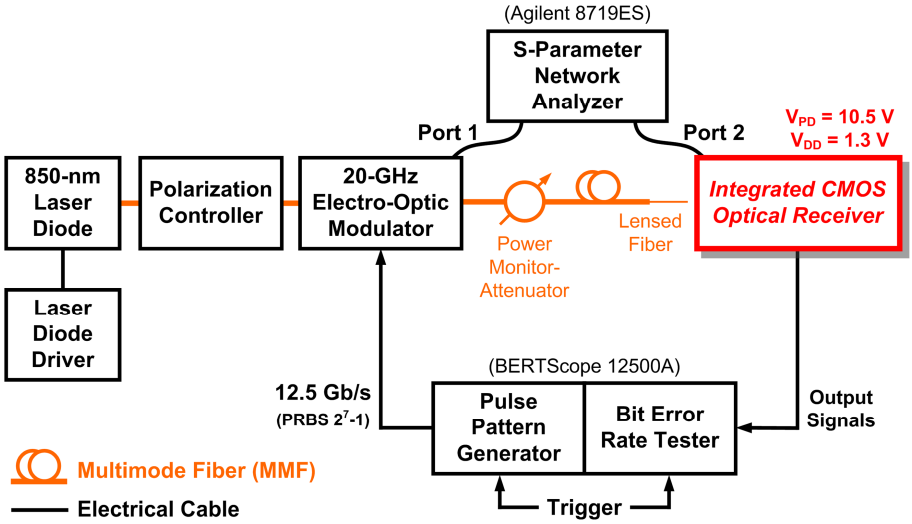

Fig. 3. Experimental setup.

Figure 3 shows the experimental setup. An 850-nm laser diode and a 20-GHz electro-optic modulator are used for optical input signal generation, and a lensed fiber is used for coupling light into the SM-APD and CMOS-Rx on a probe station.

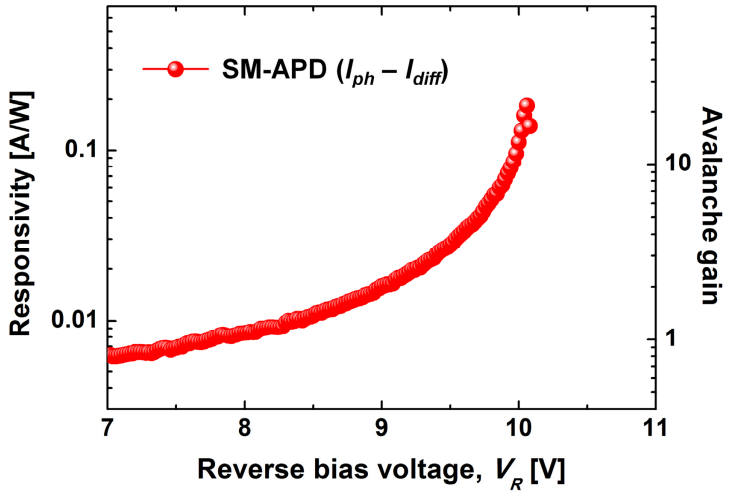

Fig. 4. Responsivity and avalanche gain of the fabricated SM-APD as a function of the reverse bias voltage.

Figure 4 shows the measured responsivity and avalanche gain of the SM-APD as a function of the reverse bias voltage. The responsivity increases with the reverse bias voltage due to the avalanche gain. The SM-APD shows maximum responsivity of about 0.18 A/W at the reverse bias voltage of about 10.05 V. The responsivity of the SM-APD is smaller than that of the CMOS-APD because a portion of its surface is covered by metal and diffusion currents are partially removed.

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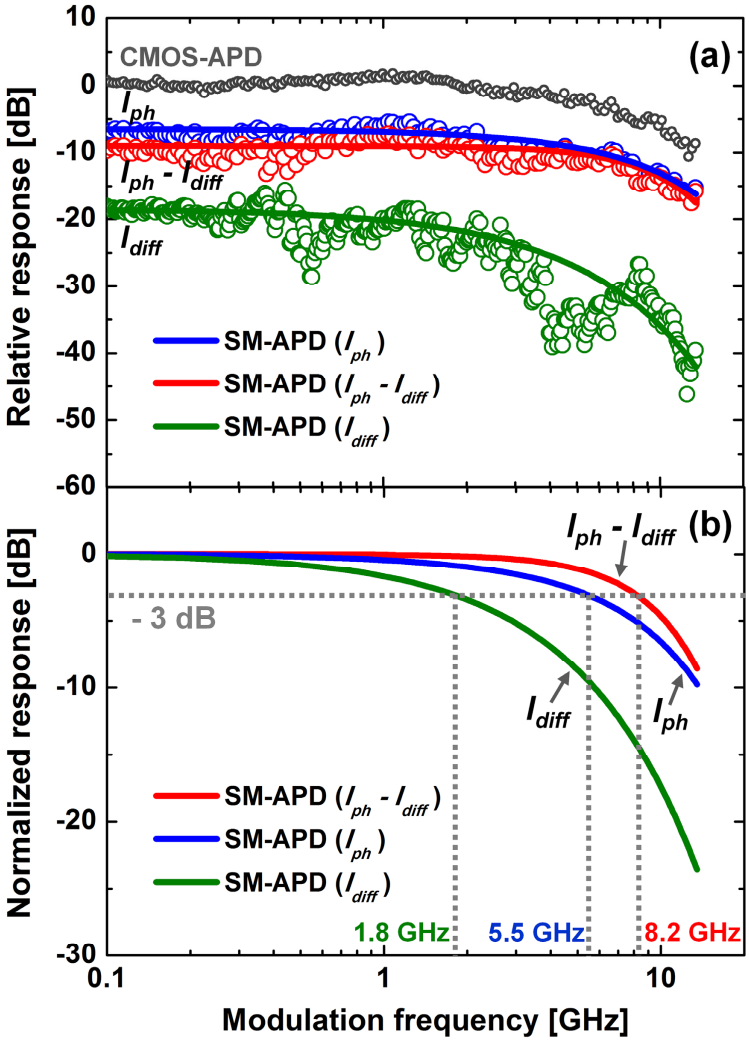

Fig. 5. (a) Measured photodetection frequency responses of the SM-APD. (b) Normalized photodetection frequency responses of the SM-APD. Hollow circles represent measured data, and solid lines represent fitted curves.

Figure 5(a) shows measured photodetection frequency responses of the SM-APD at the reverse bias voltage of 9.7 V, which gives the best bit error rate (BER) performance for the receiver. The response of I_{ph} (uncovered region) is about 6-dB lower than the response of the CMOS-APD without the light blocking metal layer since the area of the uncovered region is about half of the CMOS-APD area. This is because the photocurrent is proportional to the incident optical power, and the output electrical power is proportional to the square of the photocurrent. The response of I_{diff} (covered region), that is due to diffused photocurrents from the uncovered region, shows much less response as well as much smaller photodetection bandwidth than I_{ph}. By subtracting I_{diff} from I_{ph}, we can achieve large bandwidth as shown in Fig. 5(b) because the bandwidth-limiting diffusion components are partially removed.

For CMOS-Rx characterization, V_{PD} (Fig. 2(a)) of 10.5 V is used, which is 0.8-V larger than the reverse bias voltage, V_R, because of the TIA circuit configuration. CMOS-Rx circuits are biased with 1.3-V supply, and the total power consumption of the electronic circuits excluding the output buffer is about 72.4 mW.

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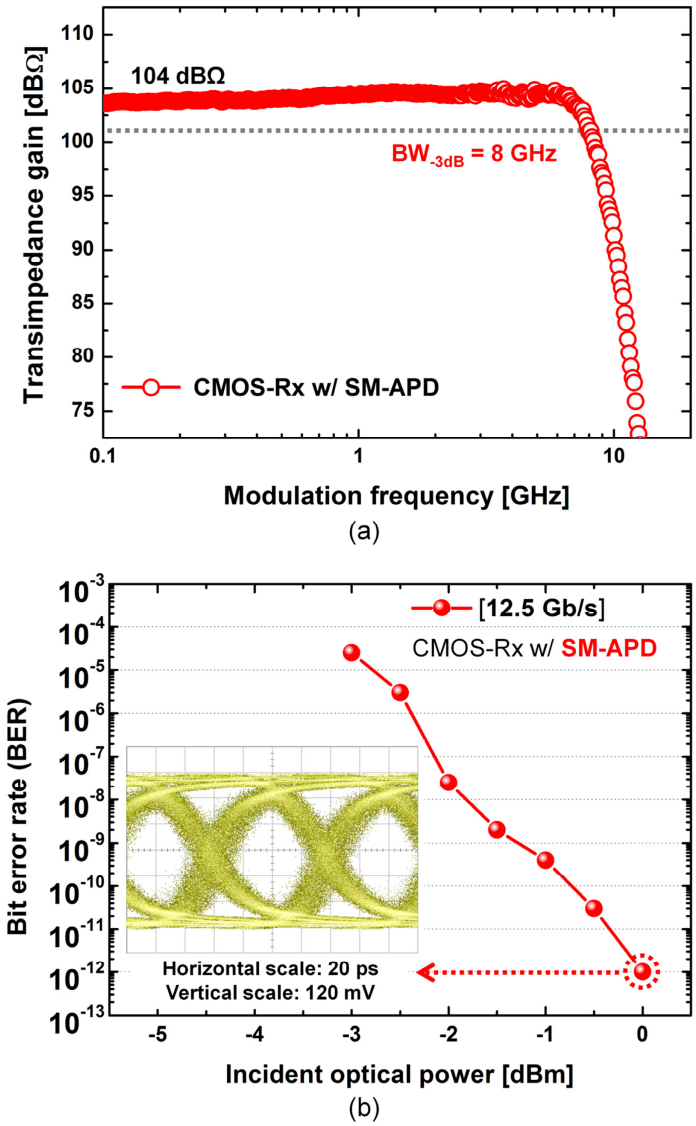

Fig. 6. (a) Normalized photodetection frequency response of the CMOS-Rx based on the SM-APD and (b) measured BER performance versus incident optical power and eye diagram for 12.5-Gb/s optical data.

Figure 6(a) shows measured photodetection frequency response of the entire CMOS-Rx. The transimpedance gain is about 104 dBΩ, and the 3-dB bandwidth is about 8 GHz. Figure 6(b) shows the measured BER performances as a function of the incident optical power for 12.5-Gb/s optical data. With our CMOS-Rx, detection of 12.5-Gb/s optical data is successfully achieved with of 10^{-12} BER. The required optical power for our receiver is quite high because a portion of its surface is covered by metal and also because it is fabricated with the standard CMOS technology, which does not allow the optimal device structure for avalanche photodetectors. Inset of Fig. 6(b) shows the corresponding eye diagram.

Table 1 shows performance summary of the CMOS-Rx based on the SM-APD and performance comparison with other CMOS-Rxs recently reported. Our CMOS-Rx achieves the highest data rate, 12.5 Gb/s, at 5.8 pJ/bit. As shown in Fig. 7, our CMOS-Rx shows superior performances to other CMOS-Rxs in terms of data rate and power efficiency.

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Table 1. Performance Summary and Comparison with other CMOS-Rxs

	[16] 10' JSSC	[18] 11' JSSC	[21] 12' JQE	This work
Technology	0.13-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.13-µm CMOS
Structure	SM-PD + TIA + EQ + LA	SM-PD + TIA + LA (9 passive inductors)	APD + TIA + EQ + LA	SM-APD + TIA + EQ + LA
Data rate	8.5 Gb/s	10 Gb/s	10 Gb/s	12.5 Gb/s
Sensitivity (BER)	–3.2 dBm (10^{-12})	–6 dBm (10^{-11})	–4 dBm (10^{-12})	0 dBm (10^{-12})
Supply voltage	1.5 V	1.8 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.5 V (PD)	1.3 V (Circuit) 10.5 V (PD)
Total power dissipation	47 mW	118 mW	66.8 mW	72.4 mW
Core chip area	0.1 mm^2	0.76 mm^2	0.26 mm^2	0.26 mm^2

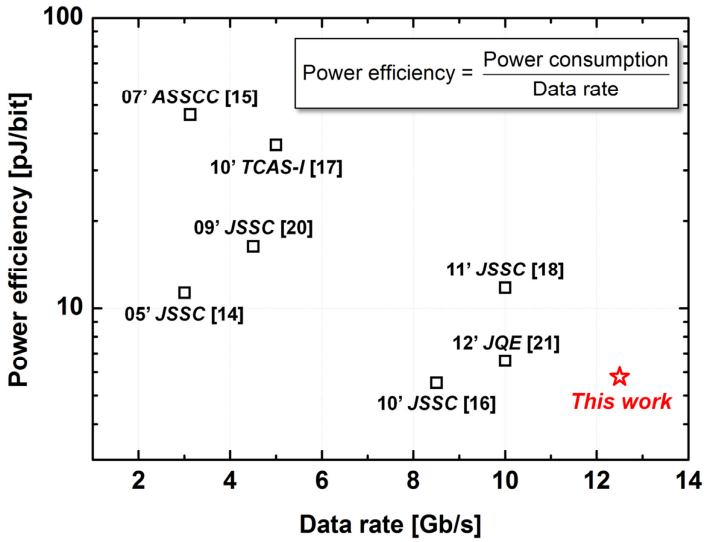

Fig. 7. Performance comparison of CMOS-Rxs in terms of data rate and power efficiency.

5. Conclusion

A 12.5-Gb/s CMOS-Rx is realized with standard 0.13-µm CMOS technology for 850-nm optical interconnect applications. The proposed CMOS-Rx shows improved performance because it has a high-speed SM-APD. With the fabricated CMOS-Rx, 12.5-Gb/s optical data are successfully detected with 10^{-12} BER at 5.8 pJ/bit. To the best of our knowledge, our CMOS-Rx achieves the highest data rate among previously reported CMOS-Rxs.

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